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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,529	06/26/2003	Francesco A. Campisano	END920030021US1	4833

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EXAMINER	
ZHAO, DAQUAN	

ART UNIT	PAPER NUMBER
2621	

NOTIFICATION DATE	DELIVERY MODE
09/03/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/607,529	CAMPISANO ET AL.	
	Examiner	Art Unit	
	DAQUAN ZHAO	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 5/18/2009 have been fully considered but they are not persuasive.

2. Applicant argues, on pages 8-9 of the remark, "decoding in a single iteration" is supported by paragraphs 37-38. However, after reviewing paragraphs 37-38 of the instant application, the examiner finds no correlation between the cited paragraphs with the claimed limitation "decoding in a single iteration", the cited passage on page 8-9 of the remark "[a]s the frames are decoded, they will be read out in order from their corresponding buffers according to display synchronization signal 162. So that the proper display order is maintained, the controller microcode will also synchronize the display pointer (not shown) to the current pointer address" only describes the display order of the frames and has nothing to do with "decoding in a single iteration".

3. Applicant also argues, on pages 9-10 of the remark, Bohnke fails to teach "decoding in a single iteration". Column 6, lines 31-38, clearly teach "...the turbo decoder 28 only performs one decoding iteration step at a time..." and lines 39-40 also recites: "Besides the means for performing at least one decoding iteration on multidimensionally coded information, e.g. the shown turbo decoder 28, the decoding apparatus according to the present invention further comprises means 32 for checking the decoded information after each decoding...If error is detected in the transmitted data d0, d1..., dN-1, a control signal is generated and fed back to the turbo decoder 28. The turbo decoder 28 comprises a trigger unit or a control unit to activate the turbo decoder

28 to perform a further decoding iteration step..." Therefore, the turbo decoder 28 only performs addition decoding when it is triggered by the error detected. When there's no error detected, the turbo decoder only performs one decoding iteration.

4. Applicant also argues, on page 10 of the remark, "the Office fail to teach or suggest how or if its turbo decoder would function in a trick play environment". The examiner disagrees. The trick mode playback of the video data have to have a video decoder, and the encoded video cannot be playback without a decoder. Therefore, the turbo decoder can be function in the trick play environment.

5. Applicant argues, on page 10-11 of the remark, "...the office relies on a passage of Kim, which the office states teaches removal of a one byte synch from the trick play data. However, as argued previously, this one byte synch is a byte in the trick play data itself and is removed from the data itself and, as such is not a signal that is within the MPEG-2 decoder. The examiner disagrees. Page 6 of the previous Office Action, the examiner has cited "column 1, lines 27-42 and column 7, lines 32-56, VLD analyzer 118 is considered to be the MPEG2 decoder. The 1-byte sync is separates by the packetizer & mapper 120 follower by the VLD decoder as shown in figure 1. It has been held that making previously separated components integral into one unit without producing any new and unexpected result involves only routine skill in the art. See In re Larson, 340 F.2d 965,968; 144 USPQ 347 349 (CCPA 1965). "

There's no new ground(s) of rejection. A copy of the previous Office Action is provided below.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

For claims 1, 8 and 14, there's no description for the newly added limitation: decoding in a single iteration.

Claims 2-7, 9-13 and 15-21 incorporated the same deficiency as set forth in claims 1, 8 and 14 above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 14 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al (US 6,473,558 B1), in view of Nagata (US 5,974,224) and further in view of Bohnke (US 6,557,139 B2).

For claim14, Wu et al teach an MPEG-2 buffer scheme for providing enhanced trick mode playback of a video stream (e.g. column 7, lines 52-59 and column 8, lines 17-28, a frame-by-frame reverse play is a type of trick mode playback, the GOP which contains I, P and B frame shown in figures 4-6 are considered to be the video stream), comprising:

a first buffer having a first pointer that is associated with a firs address, and a second buffer having a second pointer that is associated with a second address (e.g. column 8, lines 30-57, frame pointers is used to direct the decoded frame into a memory location, wherein the memory location corresponds to the "address", the F and B pointer are used for directing the I and P frames to the appropriate frame buffers),

wherein the first pointer is locked to the first buffer and the second pointer is locked to the second buffer (e.g. column 9, lines 11-24, pointers F and B points to frame buffers M1 and M2 during a cycle), and

wherein a set of frames of the video stream comprising at least one I frame and at least zero p frames is decoded for trick mode playback to the first buffer and the second buffer in a strictly alternating fashion based on a continuous swapping of the first address and the second address on a frame by frame basis (e.g. column 9, line 45-column 10, line 23, the pointers alternate between F and B pointers. as shown in figure 5, lines 525, F and B continuously swapping during each cycle to direct the I frame and

P frame to different buffer during fast reverse play, because the pointers are use to direct the decoded frame into a memory location (address). Therefore, the first address (address of F point to in a buffer) and the second address (address of B pointing to in a different buffer) are swapping continuously.

frames in the first buffer is immediately followed by a frame in the second buffer and frames in the second buffer is immediately followed by a frame in the first buffer until an end of the video stream (Column 10, lines 7-33 and figure 5 of Wu et al teach the order in which frame buffers M1, M2 and M3 are accessed, which is M1, M2 and then M3 in the first cycle, and M3, M2 and then M1 in the next cycle, Wherein M1 is followed by M2 immediately in the first cycle and M2 is followed by M1 immediately in the second cycle).

However, Wu et al fail to specify using only two buffers to reproduce the video frames; decoding in a single iteration. Nagata teaches using only two buffers to reproduce the video frames (e.g. figure 8, buffer 91 and 92). It would have been obvious to one ordinary skill in the art at the time the invention was made to modify the teaching of Wu et al using the two buffer taught by Nagata to allow ***every*** frame in the first buffer is immediately followed by a frame in the second buffer and ***every*** frame in the second buffer is immediately followed by a frame in the first buffer until an end of the video stream. Therefore, it is obvious to one ordinary skill in the art to try using only two buffers instead of three buffers in the system of Wu et al to decode video frame in the alternative fashion and reduce the size of the apparatus or the cost of the apparatus (KSR International Co. v. Teleflex Inc. (KSR), 550 U.S. ___, 82 USPQ2d 1385 (2007).

Wu et al and Nagata fail to teach decoding in a single iteration. Bohnke teaches decoding in a single iteration (e.g. abstract, "...at least one decoding iteration on multi-dimensionally coded information..." and column 6, lines 31-38). It would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate the teaching of Bohnke into the teaching of Wu et al and Nagata to enable an optimized and effective iterative decoding of multi-dimensionally coded information (e.g. Bohnke, column 3, lines 50-55).

For claim 20, Wu et al teach the set of frames are part of a group of pictures with a set of B frames (e.g. see column 5, lines 46-60 for GOPs and column 4, lines 1-5 for I P and B frames).

For claim 18, Wu et al teach the display pointer is synchronized with the first address, and wherein the decoded set of frames is read out of the first buffer and the second buffer in the alternating fashion based on the display pointer (e.g. pointers F and B are for displaying the frames).

For claim 19, Wu et al teach the first buffer is a current buffer and the second buffer is a past buffer (e.g. buffers M1 and M2 are alternating).

For claim 21, Wu et al teach a third buffer, wherein the set of frames are decoded to the first buffer, the second buffer and the third buffer in the alternating fashion based on a continuous swapping of the first address, the second address and a third address (e.g. buffer M5 is consider to be the third buffer).

5. Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13,15,16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al (US 6,473,558 B1), Nagata (US 5,974,224) and Bohnke (US 6,557,139 B2), as applied to claims 14 and 18-21 above and further in view of Kim (6,466,733 B1).

See the teaching of Wu et al, Nagata and Bohnke above.

For claims1, 2, 8, 9, 15 and 16, Wu et al, Nagata and Bohnke fail to teach disengagement of a frame synchronization signal within the MPEG-2 decoder. Kim teaches disengagement of a frame synchronization signal within the MPEG-2 decoder (e.g. column 1, lines 27-42 and column 7, lines 32-56, VLD analyzer 118 is considered to be the MPEG2 decoder. The 1-byte sync is separates by the packetizer &mapper 120 follower by the VLD decoder as shown in figure 1. It has been held that making previously separated components integral into one unit without producing any new and unexpected result involves only routine skill in the art. See In re Larson, 340 F.2d 965, 968; 144 USPQ 347, 349 (CCPA 1965). It would have been obvious for one ordinary skill in the art at the time the invention was made to incorporate the teaching of Kim into the teaching of Wu et al, Nagata and Bohnke to increase the stability of a system since Kim suggests to extract the sync block to simplify the error correction process when decoding a signal in a trick play mode (Kim, column 8, line 59-column 9, line 13).

For claim 4, Wu et al teach the first buffer is a current buffer and the second buffer is a past buffer (e.g. buffers M1 and M2 are alternating).

For claim 6, Wu et al teach the set of frames are part of a group of pictures with a set of B frames (e.g. see column 5, lines 46-60 for GOPs and column 4, lines 1-5 for I P and B frames).

For claim 3, Wu et al teach synchronizing a display pointer with the first address and reading the decoded set of frames out of the first buffer and second buffer in the alternating fashion based on the display pointer (e.g. figure 6, frames are display in a sequence using the pointers F and B alternatively).

Claims 7 and 10 is rejected for the same reasons as discussed in claim 3 above.

For claim 11, Wu et al teach the first buffer is a current buffer and the second buffer is a past buffer (e.g. buffers M1 and M2 are alternating).

For claim 12, Wu et al teach the set of frames are part of a group of pictures with a set of B frames (e.g. see column 5, lines 46-60 for GOPs and column 4, lines 1-5 for I P and B frames).

For claim 13, Wu et al teach a third buffer, wherein the set of frames are decoded to the first buffer, the second buffer and the third buffer in the alternating fashion based on a continuous swapping of the first address, the second address and a third address (e.g. buffer M5 is consider to be the third buffer).

For claims 5 and 17, Wu et al teach the first address and the second address are continuously swapped by microcode (e.g. the pointer F and B are considered to be the microcode).

There's no new ground(s) of Rejection. Accordingly, THIS ACTION IS MADE FINAL. See MPEG § 706.07 (a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136 (a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing data of this action. In the event a first reply is filed within TWO MONTHS of the mailing data of this action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period. Then the shortened statutory period will expire on the data the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing data of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the data of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daquan Zhao whose telephone number is (571) 270-1119. The examiner can normally be reached on M-Fri. 7:30 -5, alt Fri. off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tran Thai Q, can be reached on (571)272-7382. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Daquan Zhao/
Examiner, Art Unit 2621

/Thai Tran/

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